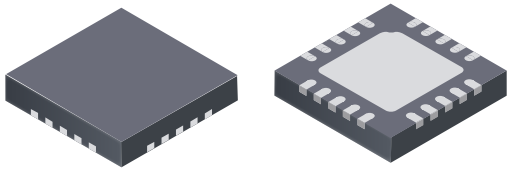
A4942

Three-Phase Sensorless Fan Driver

FEATURES AND BENEFITS

- Sensorless (no Hall sensors required)
- Closed loop speed control
- Minimal external components
- PWM speed input
- FG speed output
- Lock detection
- Soft start
- Overcurrent protection
- Soft switching for reduced audible noise

Package: 20-contact QFN (suffix ES)



Not to scale

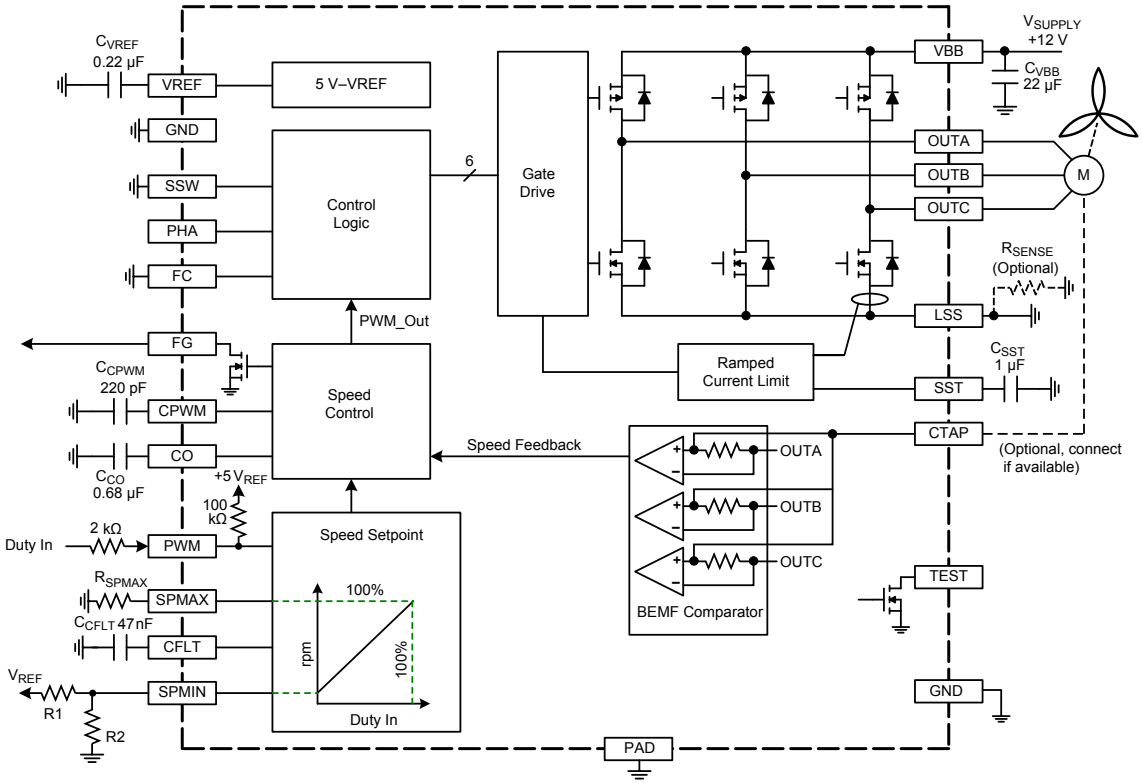
DESCRIPTION

The A4942 three phase motor driver incorporates BEMF sensing to eliminate the requirement for Hall sensors in fan applications.

A closed loop speed control system is integrated into the IC. This allows accurate setting of maximum and minimum speeds via selection of external resistors. The speed is controlled by duty cycle demand applied to the PWM input. The PWM input is allowed to operate over a wide frequency range.

Current limiting is integrated to allow saving the cost and PCB space of an external sense resistor. The current limit function includes an adjustable soft start to minimize load on the power supply while the fan is ramping up to speed.

The A4942 is supplied in a 20-contact 4 mm × 4 mm QFN package (suffix ES) with exposed pad for enhanced thermal dissipation. The package is lead (Pb) free, with 100% matte tin leadframe plating.



Functional Block Diagram

SPECIFICATIONS

SELECTION GUIDE

Part Number	Packing	Package
A4942GESTR-T	1500 pieces per 7-in. reel	20-contact QFN with exposed thermal pad

ABSOLUTE MAXIMUM RATINGS

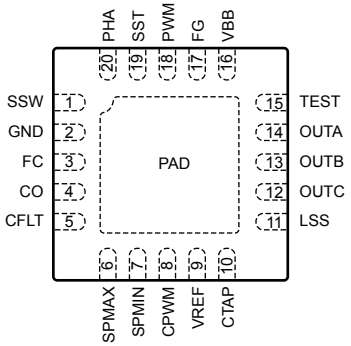
Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		16	V
Logic Input Voltage Range	V_{IN}	PWM	–0.3 to 6	V
Logic Output	V_O	FG	V_{BB}	V
Output Current	I_{OUT}	Locked rotor condition, internally limited	1.6	A
		Duty Cycle = 100%	800	mA
Operating Ambient Temperature	T_A	G temperature range	–40 to 105	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions: see application information

Characteristic	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	2-sided PCB with 0.60 in^2 copper	75	°C/W
		4-layer PCB based on JEDEC standard	37	°C/W

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PINOUT DIAGRAM AND TERMINAL LIST



Pin-out Diagram

Terminal List Table

Number	Name	Function
1	SSW	Soft switch duty cycle adjust
2	GND	Ground
3	FC	Capacitor to set startup oscillator
4	CO	Speed control loop comparator capacitor
5	CFLT	PWM filter capacitor
6	SPMAX	Speed curve set maximum
7	SPMIN	Speed curve set minimum
8	CPWM	Set motor PWM frequency
9	VREF	Reference voltage output
10	CTAP	Motor terminal center tap
11	LSS	Ground
12	OUTC	Motor terminal phase C
13	OUTB	Motor terminal phase B
14	OUTA	Motor terminal phase A
15	TEST	Test use only – open circuit
16	VBB	Input supply
17	FG	Speed output signal
18	PWM	Logic input – speed (demand 1 to 100 kHz)
19	SST	Soft start adjustable current limit
20	PHA	Logic input – 3 state select
–	PAD	Exposed thermal pad

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ELECTRICAL CHARACTERISTICS: Valid at T_A = 25°C, V_{BB} = 12 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Voltage Range	V_{BB}		5	–	16	V
VBB Supply Current	I_{BB}		–	13.5	15	mA
Total Driver On-Resistance (Sink + Source)	$R_{DS(on)}$	I_{OUTx} = 800 mA, T_J = 25°C, V_{BB} = 12 V	–	1	1.2	Ω
Overcurrent Threshold	I_{CL}	LSS = GND, T_J = 25°C	1.3	1.45	1.6	A
		LSS = GND, T_J = –40°C to 105°C	1.1	–	1.8	A
Overcurrent Threshold Voltage	V_{OCL}		185	200	215	mV
PWM Low Level	V_{IL}		0	–	1	V
PWM High Level	V_{IH}		2	–	5.5	V
Input Hysteresis	V_{HYS}		–	300	–	mV
Logic Input Current	I_{IN}	PWM pin, V_{IN} = 0 V	–	–50	–	µA
Output Saturation Voltage (FG and TEST pins)	V_{SAT}	I_{FG} = 5 mA	–	–	0.3	V
FG Output Leakage	I_{FG}	V_{FG} = 16 V	–	–	1	µA
Lock Protection	t_{ON}		1.35	1.5	1.65	s
	t_{OFF}		9	10	11	s
Lock Ratio	t_{OFF} / t_{ON}		6.33	6.67	7	–
Startup Oscillation Time	t_{FC}	Relative to target, C = 47 nF	–20	–	20	%
Soft Start Time	t_{SST}	Relative to target, C = 1 µF	–20	–	20	%
VBB Pin Undervoltage Lockout (UVLO)	V_{BBUVLO}	V_{BB} rising	4.5	4.75	4.95	V
VBB Pin UVLO Hysteresis	$V_{BBUVLOHYS}$		100	200	300	mV
Speed Setpoint	f_{SET}	R_{SPMAX} = 20 kΩ, PWMOUT = 20% to 100%	–5	–	5	%
		R_{SPMAX} = 20 kΩ, PWMOUT = 10% to 20%	–10	–	10	%
Internal PWM Frequency	f_{PWM}	C_{CPWM} = 220 pF	55	64	73	kHz
VREF Output Voltage	V_{REF}	I_{VREF} = 0 to 5 mA, V_{BB} = 12 V	4.8	5	5.2	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	T_{JHYS}	Recovery = T_{JTSD} – T_{JHYS}	–	20	–	°C

NOTE 1: Specified limits are tested at a single temperature and assured across the operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

Lock Detect Valid commutation signals must be detected to ensure the motor is not stalled. If a valid FG signal is not detected for 1.5 s, the outputs will be disabled for 10 s before an auto-restart is attempted.

VREF Reference voltage output used to bias external resistor dividers. External current draw should be no more than 5 mA. V_{REF} supply must be decoupled with a 0.22 µF ceramic capacitor.

FG Open drain output that provides speed information to the system.

Current Limit During a locked rotor condition, the current will ramp up to the internal current limit. Load current is monitored on the low-side MOSFET. If the current reaches the Overcurrent Threshold, I_{CL}, the drivers will be chopped at a frequency set by C_{PWM}.

Optionally, current limit can be set as:

$$Current\ Limit = 200\ mV / R_{SENSE}$$

where R_{SENSE} is an optional external component on the LSS pin.

If it is preferable to save expense and the PCB space of an external component, connect LSS to GND. This sets the current limit to the internal threshold of 1.45 A typical. Using an external resistor can only lower the current limit below the internal threshold.

PWM Input The PWM pin is the speed command input. The input frequency can be in the range from 1 to 100 kHz.

If PWM is left open circuit, the motor will run at maximum demand.

CPWM The internal PWM frequency, f_{PWM}, is selected via an external capacitor on the CPWM pin. The recommended range is 20 to 80 kHz, calculated as:

$$f_{PWM} = 1.41 \times 10^{-5} / C_{PWM}$$

CTAP Connection pin for motor center-tap if available. If not available (such as with delta type motors), the null point will be generated internally.

CFLT Terminal for an external capacitor to filter PWM input, set based on PWM input frequency. C_{FLT} has a typical value of 47 nF for a 56 kHz signal input at the PWM pin.

Soft Start The soft start function is controlled by an external capacitor on the SST pin. Typically the motor speed will limit the current, as BEMF builds up before the current limit is reached. The current limit is ramped in a linear fashion, from close to zero amperes to the current limit value. C_{SST} should be in the range from 100 nF to 2.2 µF, and the resulting soft start period can be calculated as:

$$T_{SST} = 5 \times 10^{6} \times C_{SST}$$

FC Analog input terminal for external capacitor to set startup commutation time:

$$T_{FC} = 1 \times 10^{6} \times C_{FC}$$

For FC connected to GND, t_{FC} is 50 ms.

PHA Phase Advance input, sets the internal lead angle according to the external connection as follows:

Table 1: PHA Pin Connections

PHA Pin Connection	Electrical Degrees
GND	24
VREF	6
Open	15

Lead angle adjustment advances the applied voltage relative to rotor position.

TEST Open drain output for test use only.

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Soft Switch A resistor divider from VREF to GND sets the soft switching characteristic. The voltage at the SSW pin sets the range of soft switching, as shown in Figure 1.

By connecting SSW to GND the nominal Soft Switching value of 78% can be used, while saving external component cost and PCB space. Note: Soft switching should be tested in the application at maximum open loop speed. If the motor stalls, decrease the % Soft Switching value.

R_{SPMAX} Connect external resistor to GND to set motor speed at 100% demand. Select the resistor value as:

$$\text{Maximum Speed (rpm)} = \frac{4 \times 10^8}{R_{SPMAX}}$$

where he relationship of speed to R_{SPMAX} is shown in Figure 2.

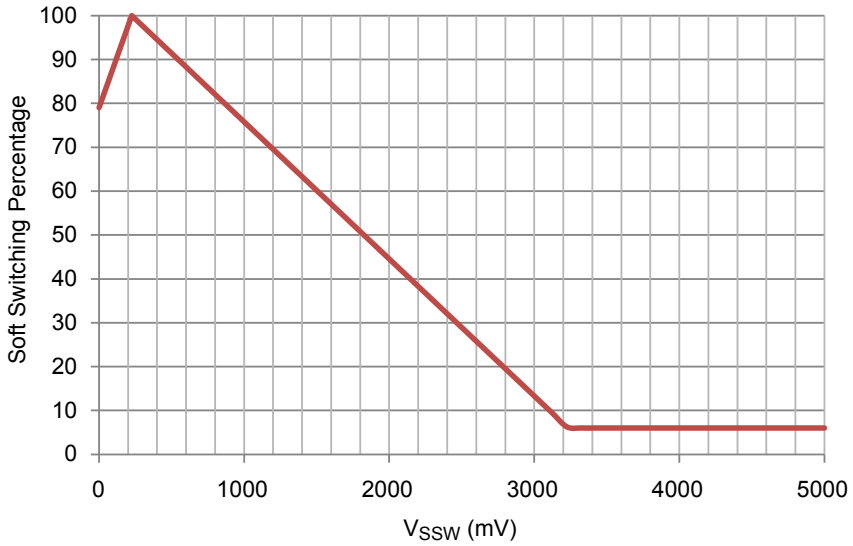


Figure 1: Soft Switching Percentage as a Function of Voltage on SSW Pin

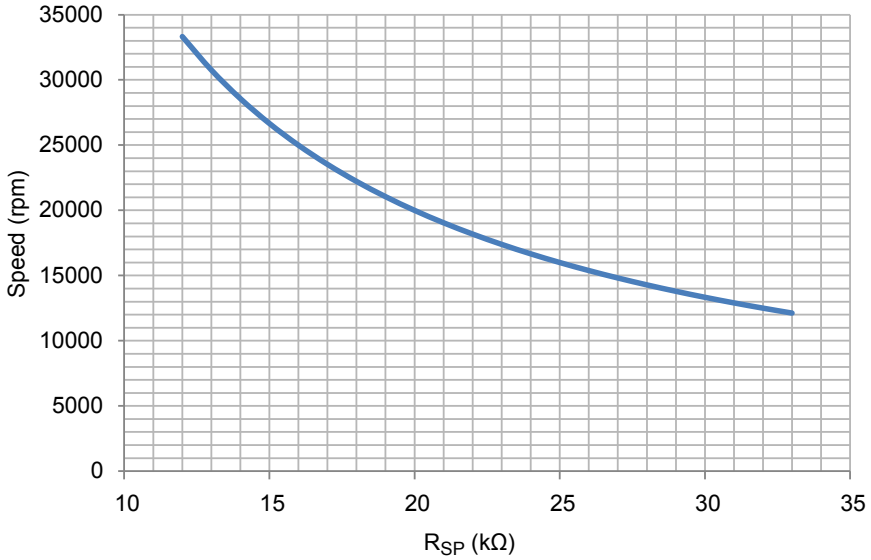


Figure 2: Commutation Speed as a Function of Resistor Value on SPMAX Pin

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APPLICATION INFORMATION

Closed Loop Speed Control System

The VREF, SPMIN and SPMAX pins are used to select the end-points of the linear speed curve characteristic (4-pole motor).

Referring to Figure 3, at startup, speed demand is controlled by V_{REF}.

Given that:

$$Maximum\ Speed\ (rpm) = 4 \times 10^8 / R_{SPMAX}$$

then:

$$Minimum\ Speed\ (rpm) = Maximum\ Speed\ (rpm) \times (5/3) \times R_2 / (R_1 + R_2)$$

$R_1 + R_2$ should be set close to 25 kΩ.

At start-up speed demand is connected to VREF. As soon as speed exceeds the target speed, the speed demand control switches to the output of the frequency locked loop. The C_{CO} value, an external capacitor on the CO pin, sets the bandwidth of speed control loop. C_{CO} is charged or discharged based on the comparison of the falling edge of f_{OUT} and f_{SET}. The typical value is 0.68 µF.

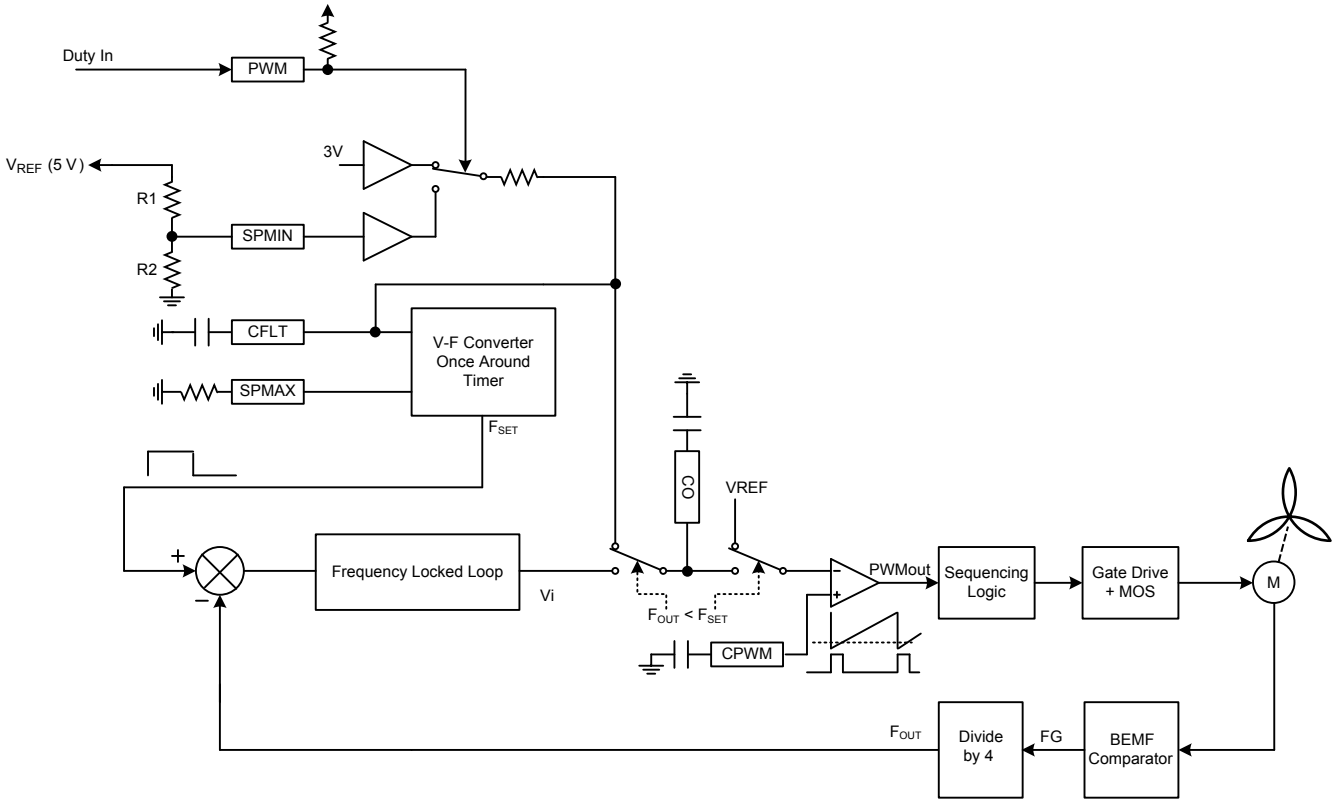


Figure 3: Equivalent Circuit of Closed Loop Control System

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Open Loop Speed Control System

An alternative, open loop control system can be applied, as shown in figure 4.

The closed loop speed control system can be disabled by connecting SPMAX to VREF. In this case, V_{CFLT} will be compared to the C_{PWM} sawtooth waveform to create the PWM output duty applied to the motor. (The C_{CO} capacitor is not required.) This configuration is shown in figure 5.

Larger C_{FLT} capacitor values can be used to slow down response in the case of large duty changes expected at the PWM input.

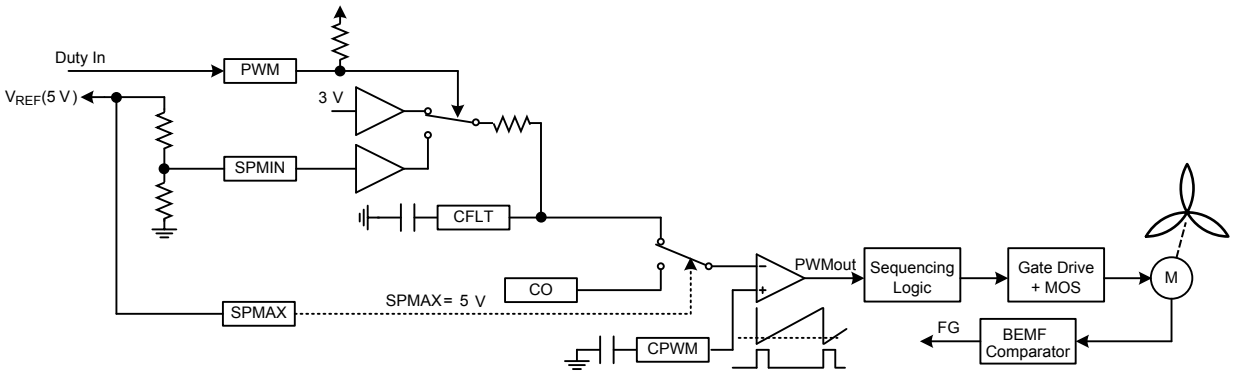


Figure 4: Equivalent Circuit of Open Loop Control System

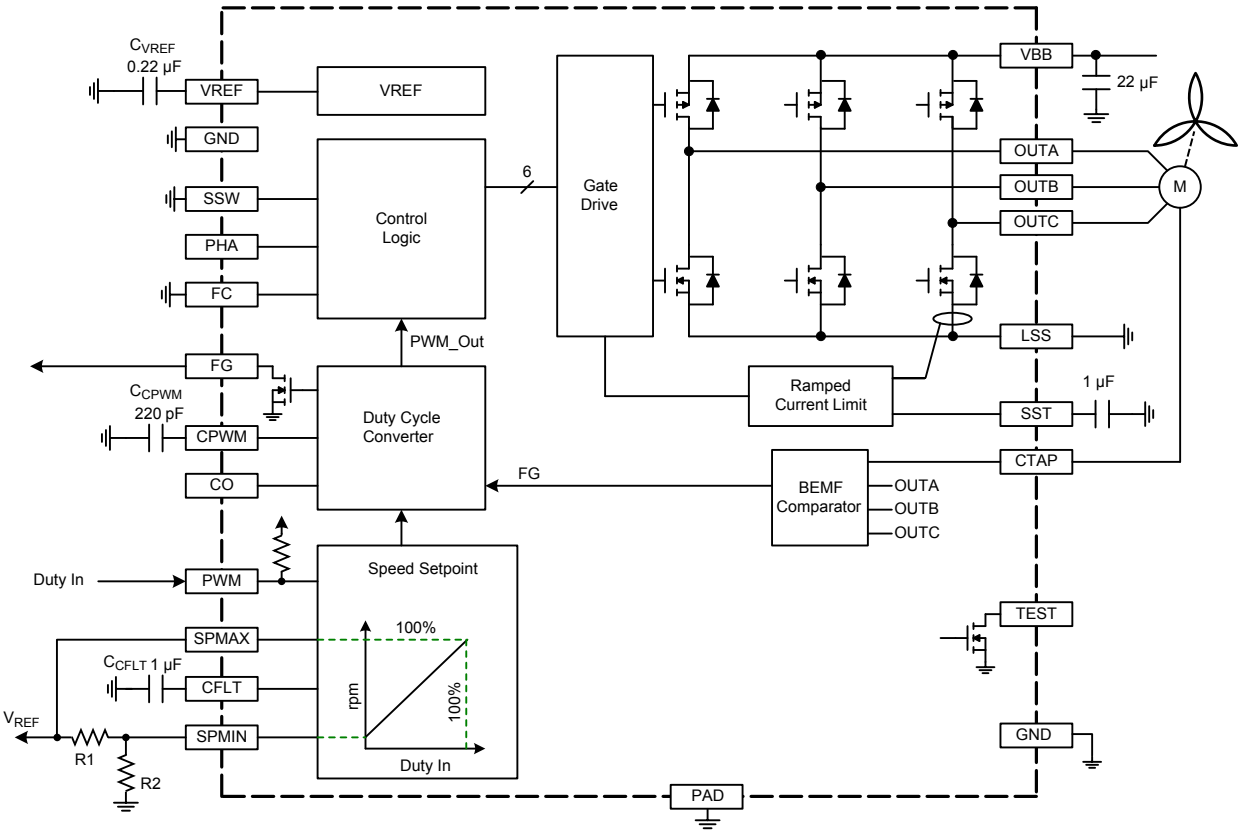


Figure 5: Functional Block Diagram Demonstrating Implementation of Open Loop Control

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Layout Notes

A typical layout is illustrated in figures 6 and 7. Recommended component values for this layout are provided in the table.

The following guidelines for PCB layout should be observed:

- Place C_{VREF} and C_{CPWM} as close as possible to the IC
- Route high impedance signal traces (CO, CFLT, and SST) away from switching nodes (OUTA, OUTB, OUTC, and CTAP)
- Connect GND and LSS directly to the exposed pad under the IC
- Utilize the ground plane on the bottom side of the PCB under the IC for low impedance returns to C_{VBB} and the power connector

Table 2: Recommended External Components

Symbol	Value	Note
C_{FC}	Connect to GND	Only required if start-up problems found
C_{CFLT}	47 nF X5R / 6.3 V	
C_{CO}	0.68 µF X5R / 6.3 V	0.68 µF is the minimum value
C_{CPWM}	220 pF X5R / 6.3 V	Sets motor PWM to 64 kHz
C_{SST}	1 µF X5R / 6.3 V	
C_{VBB}	10 to 22 µF X5R / 25 V	
C_{VREF}	0.22 µF X5R /10 V	
R_{SPMAX}	10 to 50 kΩ, 1%	Select for design maximum speed
R_{SPMIN} (R1 and R2)	1%	R1 plus R2 close to 25 kΩ total

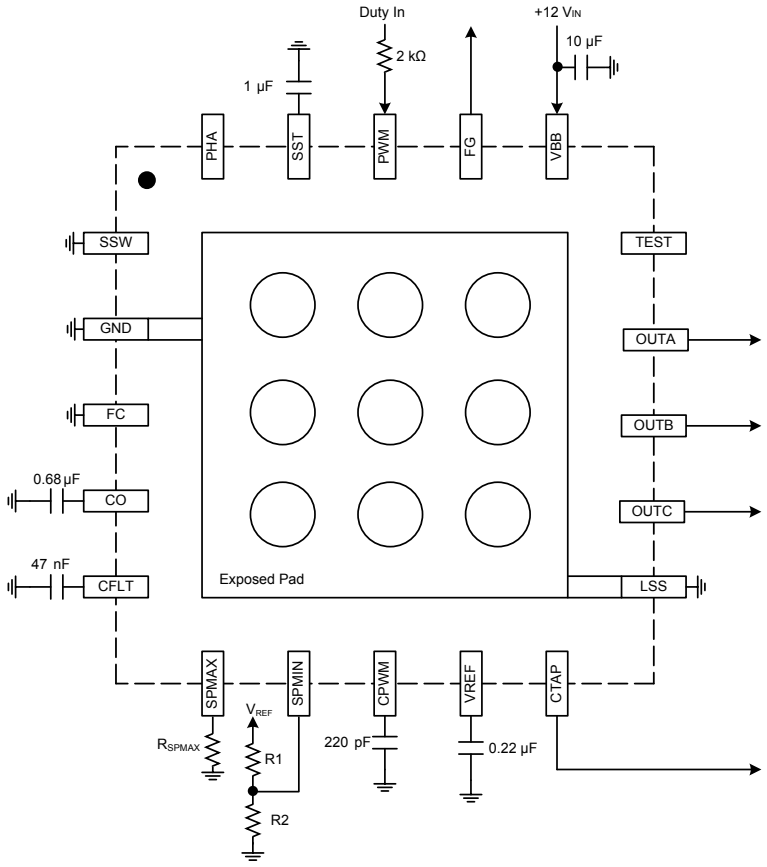


Figure 6: Typical PCB Layout

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Fan System

A typical integrating into a fan system is shown in figure 7.

Optional External Components

Typically a 4-pin connector is used to interface the system to a fan module and the A4942.

- It may be a requirement in the end application to ensure these pins survive reverse polarity connection or incorrect application of signals during the fan test process.
- D1 can be added to handle the requirement or reverse polarity connection. D1 should be a low V_f, 2 A/20 V rated component. Adding D1 will reduce efficiency and maximum speed due to the voltage drop and power loss.
- If D1 is used, then typically a clamp diode (ZD) is required to prevent voltage transients from exceeding the maximum rating to the IC. When the fan is turned off, due to the inductance of the load, the current path is back into the C_{VBB} capacitor, because D1 prevents flow back towards the 12 V supply capacitor. V_{BB} overshoot will result until the energy in the load is dissipated.
- ZD is required to clamp below the VBB pin ESD structure breakdown (approximately 20 V). If the energy stored in inductance is low enough, C_{VBB} can be increased, to lower the overshoot to a safe level, and ZD would not be required.
- Including R_{PWM} is recommended to isolate the PWM pin from the external world. The maximum rating of the PWM pin is 6 V. However, including R_{PWM} would limit the current in case of an accidental connection to VBB. With this current limit, the PWM pin ESD diode would break down at 6.5 V. The IC would not be damaged with less than 8 mA bias into the pin. 2 kΩ is the recommended value.

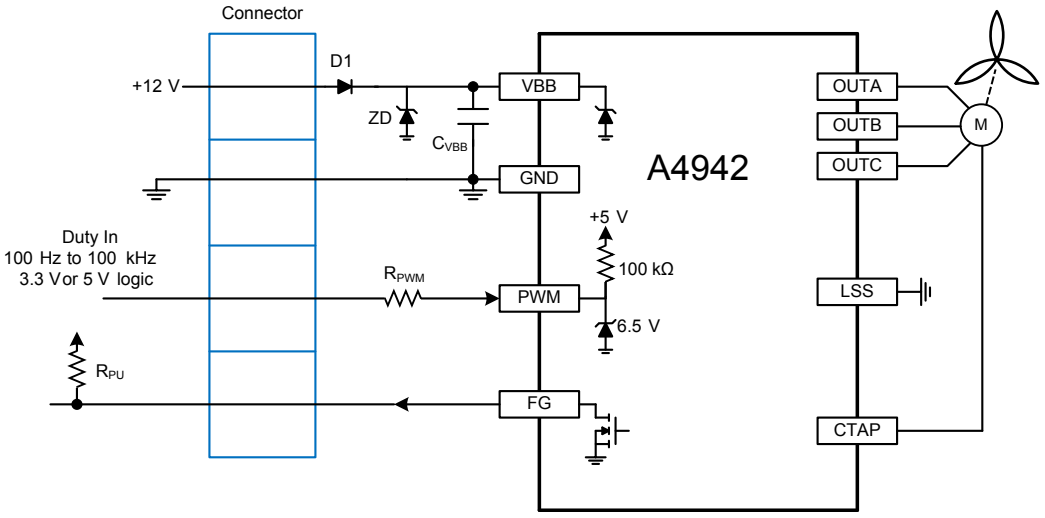


Figure 7: Typical Fan System Configuration

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PIN STRUCTURES

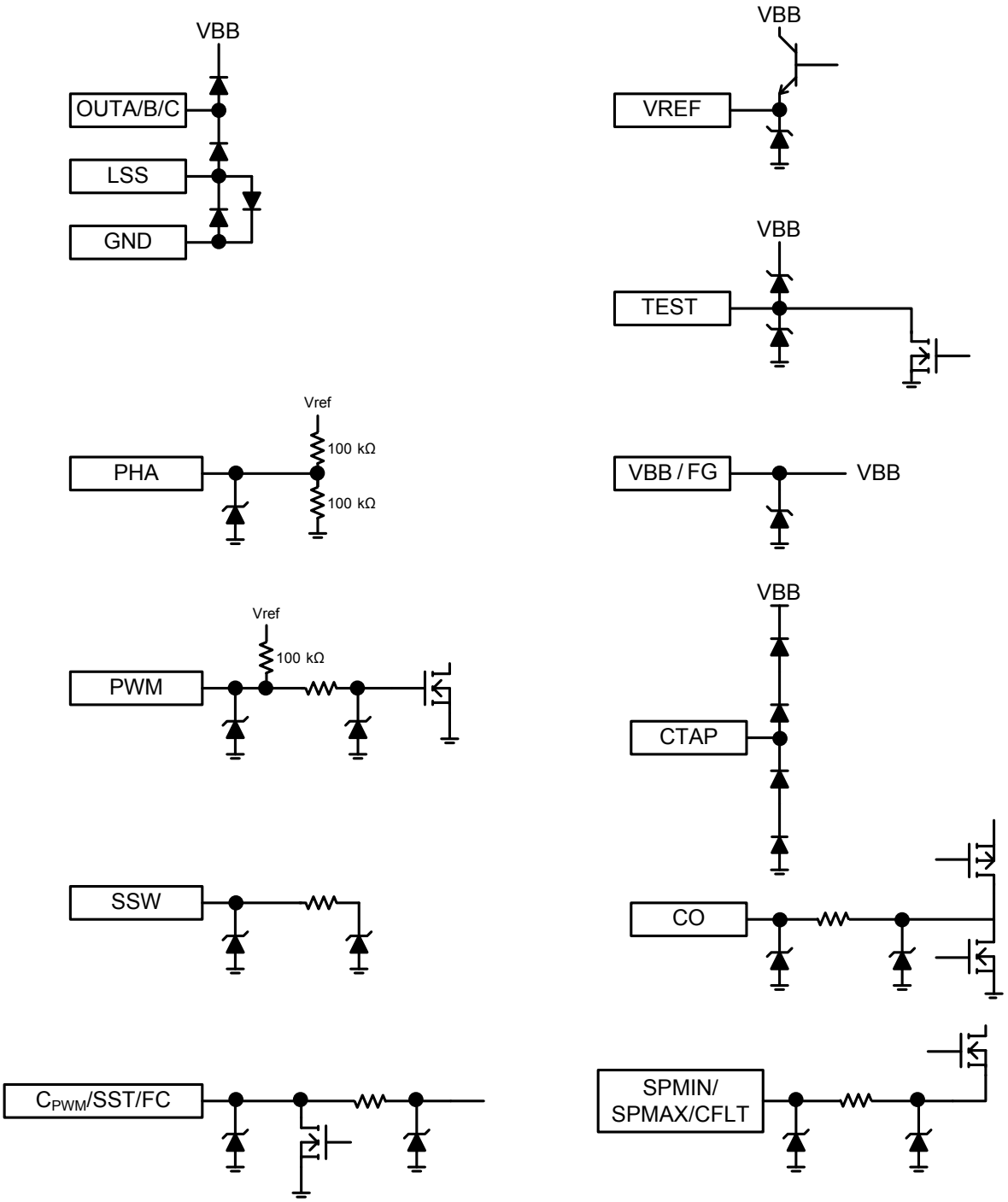


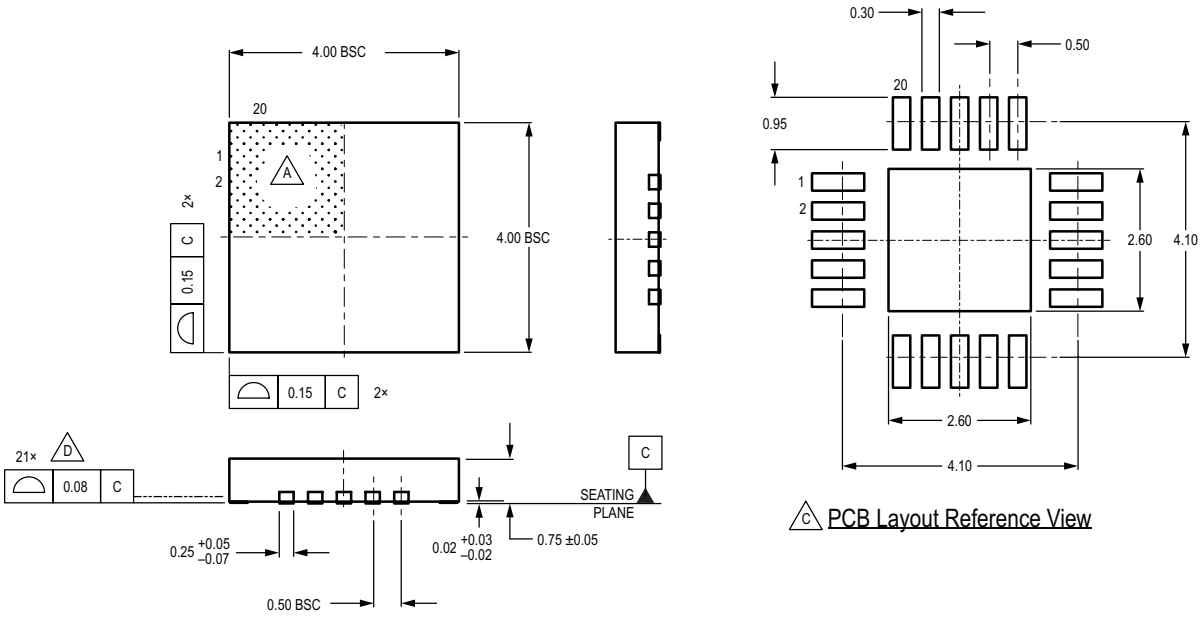
Figure 8: Pin Structures

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PACKAGE OUTLINE DIAGRAM

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD, excluding pad)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Figure 9:Package ES, 20-Pin QFN with Exposed Thermal Pad

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Revision History

Number	Date	Description
4	July 25, 2019	Minor editorial updates; initial release to web
5	July 27, 2021	Updated package drawing (page 12)

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